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EXAMINER	
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ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,912	STEISS, DONALD E.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-27,30-38 and 41-48* is/are rejected.

7)☒ Claim(s) *8,9,28,29,39 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-48 are pending.

2. The office acknowledges the following papers:

Drawings, claims, and arguments filed 7/10/2006

Withdrawn objections and rejections

3. The specification objections have been withdrawn.

4. The drawings objections have been withdrawn due to amendment to figure 7.

New Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1 and 16 recites the limitation "the traffic mode" in lines 8 and 7-8 of the claims respectfully. There is insufficient antecedent basis for this limitation in the claim.

7. Appropriate correction is required.

New Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 13-16, 21, 30-32, 41-43, and 47 are rejected under 35 U.S.C. §103(a) as being unpatentable over Joy et al. (U.S. 6,507,862), in view of Ebner et al. (U.S. 6,928,525) and Yu et al. (U.S. 6,345,345).

10. As per claim 1:

Joy disclosed a processing unit, comprising:

A plurality of processor clusters, each processor cluster having an output to send a signal representing instruction requests, an instruction request responsive to a cache miss by a processing unit within the processor clusters (Joy: Figure 11 elements 1102 and 1104, column 23 lines 23-35 and lines 54-67)(Elements 1102 and 1104 are the processing clusters. They have the ability to output a request to the arbiter via element 1122 and 1152. The requests to the arbiter are the result of a cache miss.);

An instruction request arbiter, having an input coupled to the outputs of the plurality of processor clusters, the instruction request arbiter controlling access of the plurality of processor clusters to submit instruction requests (Joy: Figure 11 element 1125, column 23 lines 23-35)(An instruction request is a request to obtain instructions from an external source to the processing cluster. The arbiter controls the request for data from the external cache. It would have been obvious to one of ordinary skill in the art that the L2$ stores data that can be either operands or instructions.); and

An instruction memory, having an input coupled to a first output of the instruction request arbiter, the instruction memory sending a signal representing instruction data to the plurality of processor clusters responsive to receiving non-conflicting instruction requests from the instruction request arbiter (Joy: Figure 11 element 1124, column 23

lines 23-35 and lines 54-67)(The instruction requests are sent back to the processor clusters through the arbiter.).

Joy failed to teach the instruction request arbiter also detecting conflicts between the instruction requests and the instruction request arbiter controlling access of the plurality of processor clusters to submit instruction requests by broadcasting the traffic mode to the plurality of processor clusters.

However, Ebner disclosed the instruction request arbiter also detecting conflicts between the instruction requests (Ebner: Figure 4 element 404, column 3 lines 56-63 and column 5 lines 16-20)(The arbiter, element 101, detects conflicts between multiple requests.).

The L2 cache is a 4 way set associative cache (Joy: Column 23 lines 30-35). The advantage of an arbiter having the ability to detect cache request conflicts is to allow one instruction request access to the cache because only one request will be able to go through at once. One of ordinary skill in the art would have been motivated to make sure that one request had the ability to fetch instructions from the L2 cache. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement an arbiter that can detect cache conflicts for the advantage of ensuring a single request was able to fetch instruction from the L2 cache.

Joy and Ebner failed to teach the instruction request arbiter controlling access of the plurality of processor clusters to submit instruction requests by broadcasting the traffic mode to the plurality of processor clusters.

However, Yu disclosed the instruction request arbiter controlling access of the

plurality of processor clusters to submit instruction requests by broadcasting the traffic mode to the plurality of processor clusters (Yu: Figure 4, column 7 lines 20-53)(The traffic mode is determined on whether the number of transfers are limited or not).

The advantage of the arbitration system of Yu is that data traffic conditions can be monitored dynamically (Yu: Column 1 lines 46-48). Control values can be set that limits the amount of traffic of data transfers in a given clock cycle (Yu: Column 2 lines 6-13). One of ordinary skill in the art at the time of the invention would have implemented the arbitration system of Yu for the advantage of dynamically monitoring data traffic to the system's memory. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement Yu's arbitration system for the advantage of dynamically monitoring and determining the amount of data traffic allowable to the system's memory.

11. As per claim 13:

Joy, Ebner, and Yu disclosed the processing unit of claim 1, wherein the plurality of processor clusters comprise a plurality of processing units (Joy: Figure 12 elements 1232-1246, column 26 lines 20-32)(The processing clusters 1102 and 1104 show the plurality of processing units in figure 12.), each of the processing units submitting requests responsive to a traffic mode (Yu: Figure 4, column 7 lines 20-53)(The traffic mode is determined on whether the number of transfers are limited or not).

12. As per claim 14:

Joy, Ebner, and Yu disclosed the processing unit of claim 1, wherein at least one of the plurality of processor clusters comprises at least one multithreaded processing

unit capable of processing a plurality of instruction threads (Joy: Figure 11 elements 1104, 1140, and 1142, column 24 lines 5-27)(The processing cluster is a processing unit capable of processing two instruction threads.), each of the plurality of threads submitting requests responsive to a traffic mode (Yu: Figure 4, column 7 lines 20-53)(The traffic mode is determined on whether the number of transfers are limited or not).

13. As per claim 15:

Joy, Ebner, and Yu disclosed the processing unit of claim 14, wherein the at least one multithreaded processing unit comprises a plurality of multithreaded processing cores (Joy: Figure 11 elements 1104, 1140, and 1142, column 24 lines 5-27)(The processing cluster is a processing unit capable of processing a two instruction threads. Each thread has it's own pipeline core and inherent that each can request data from an external cache.), each of the plurality of multithreaded processing cores submitting requests responsive to a traffic mode (Yu: Figure 4, column 7 lines 20-53)(The traffic mode is determined on whether the number of transfers are limited or not).

14. As per claim 16:

Claim 16 essentially recites the same limitations of claim 1. Therefore, claim 16 is rejected for the same reasons as claim 1.

15. As per claim 21:

Claim 21 essentially recites the same limitations of claim 1. Claim 21 additionally recites the following limitations:

Determining a traffic mode for the plurality of processor clusters, an instruction

request responsive to a cache miss by a processing unit within a processor cluster (Yu: Figure 4, column 7 lines 20-53)(The traffic mode is determined on whether the number of transfers are limited or not.);

Controlling submissions of instruction requests by each of the processing units by broadcasting the traffic mode to the plurality of processor clusters (Yu: Figure 4, column 7 lines 20-53)(The combination of Yu, with Joy and Ebner results in an arbiter that controls traffic between processing clusters. Yu disclosed implementing a limit of transfers from one space to another, and implementing a wait signal if the transfer limit is reached, which stops all traffic from one space to another. Thus, the combination results in the arbiter controlling data transfers according to the traffic mode of either transferring data or waiting because data transfers have exceeded a limit.);

The advantage of the arbitration system of Yu is that data traffic conditions can be monitored dynamically (Yu: Column 1 lines 46-48). Control values can be set that limits the amount of traffic of data transfers in a given clock cycle (Yu: Column 2 lines 6-13). One of ordinary skill in the art at the time of the invention would have implemented the arbitration system of Yu for the advantage of dynamically monitoring data traffic to the system's memory. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement Yu's arbitration system for the advantage of dynamically monitoring and determining the amount of data traffic allowable to the system's memory.

16. As per claim 30:

Claim 30 essentially recites the same limitations of claim 14. Therefore, claim 30 is rejected for the same reasons as claim 14.

17. As per claim 31:

Claim 31 essentially recites the same limitations of claim 15. Therefore, claim 31 is rejected for the same reasons as claim 15.

18. As per claim 32:

Claim 32 essentially recites the same limitations of claim 43. Therefore, claim 32 is rejected for the same reasons as claim 43.

19. As per claim 41:

Claim 41 essentially recites the same limitations of claim 13. Therefore, claim 41 is rejected for the same reasons as claim 13.

20. As per claim 42:

Claim 42 essentially recites the same limitations of claim 14. Therefore, claim 42 is rejected for the same reasons as claim 14.

21. As per claim 43:

Joy disclosed an instruction request arbiter, comprising:

A memory access module, having an input coupled to receive signals representing a plurality of instruction requests, the memory access module forwarding instruction requests (Joy: Figure 11 element 1125, column 23 lines 23-35 and 54-67)(The arbiter forwards requests for data to the external cache.);

An instruction request responsive to a cache miss by a processor within the processor cluster (Joy: Figure 11 elements 1102 and 1104, column 23 lines 23-35 and

lines 54-67)(Elements 1102 and 1104 are the processing clusters. They have the ability to output a request to the arbiter via element 1122 and 1152. The requests to the arbiter are the result of a cache miss.);

Joy failed to teach a bus access module, having an input coupled to receive signals representing a plurality of instruction request indications, the bus access module determining a traffic mode to control submissions of instruction requests by processor clusters; and the memory access module forwarding non-conflicting instruction requests.

However, Ebner disclosed the memory access module forwarding non-conflicting instruction requests (Ebner: Figure 4 element 405, column 3 lines 56-63 and column 5 lines 21-25)(The arbiter, element 101, detects conflicts between multiple requests.).

The L2 cache is a 4 way set associative cache (Joy: Column 23 lines 30-35). The advantage of an arbiter having the ability to detect cache request conflicts is to allow one instruction request access to the cache because only one request will be able to go through at once. One of ordinary skill in the art would have been motivated to make sure that one request had the ability to fetch instructions from the L2 cache. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement an arbiter that can detect cache conflicts for the advantage of ensuring a single request was able to fetch instruction from the L2 cache.

Joy and Ebner failed to teach a bus access module, having an input coupled to receive signals representing a plurality of instruction request indications, the bus access module determining a traffic mode to control submissions of instruction requests by

processor clusters.

However, Yu disclosed a bus access module, having an input coupled to receive signals representing a plurality of instruction request indications, the bus access module determining a traffic mode to control submissions of instruction requests by processor clusters, the bus access module controlling submission of instruction request by broadcasting the traffic mode to the plurality of processor clusters (Yu: Figure 4, column 7 lines 20-53)(The traffic mode is determined on whether the number of transfers are limited or not. The combination of Yu, with Joy and Ebner results in an arbiter that controls traffic between processing clusters. Yu disclosed implementing a limit of transfers from one space to another, and implementing a wait signal if the transfer limit is reached, which stops all traffic from one space to another. Thus, the combination results in the arbiter controlling data transfers according to the traffic mode of either transferring data or waiting because data transfers have exceeded a limit.).

The advantage of the arbitration system of Yu is that data traffic conditions can be monitored dynamically (Yu: Column 1 lines 46-48). Control values can be set that limits the amount of traffic of data transfers in a given clock cycle (Yu: Column 2 lines 6-13). One of ordinary skill in the art at the time of the invention would have implemented the arbitration system of Yu for the advantage of dynamically monitoring data traffic to the system's memory. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement Yu's arbitration system for the advantage of dynamically monitoring and determining the amount of data traffic allowable to the system's memory.

22. As per claim 47:

Claim 47 essentially recites the same limitations of claim 13. Therefore, claim 47 is rejected for the same reasons as claim 13

23. Claims 2-4, 7, 17, 19, 22-24, 27, 33-34, 37-38, and 44-46 are rejected under 35 U.S.C. §103(a) as being unpatentable over Joy et al. (U.S. 6,507,862), in view of Ebner et al. (U.S. 6,928,525) and Yu et al. (U.S. 6,345,345), further in view of Lentz et al. (U.S. 6,219,763).

24. As per claim 2:

Joy, Ebner, and Yu disclosed the processing unit of claim 1.

Joy, Ebner, and Yu failed to teach wherein the instruction request arbiter resolves conflicts between instruction requests having different priority indications by selecting an instruction request with the highest priority.

However, Lentz disclosed wherein the instruction request arbiter resolves conflicts between instruction requests having different priority indications by selecting an instruction request with the highest priority (Lentz: Figure 7, column 14 lines 32-67 continued to column 15 lines 1-2 and 13-27)(The request with the highest priority is granted over a lower priority request.).

Joy, Ebner, and Yu disclosed an arbiter that will pick between multiple requests for data from the external cache. The data could be either instruction operands or instructions. However, Joy, Ebner, and Yu didn't disclose the process of how the arbitration is done. Lentz disclosed an arbiter that specifies how the arbitration is done

between multiple requests. One of ordinary skill in the art would have been motivated to add a process of arbitration to the arbiter of Joy to be able to choose between multiple requests. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement an arbiter with a process of arbitration so that a request could be chosen among multiple requests.

25. As per claim 3:

Joy, Ebner, Yu, and Lentz disclosed the processing unit of claim 2, wherein a high priority is indicative of an instruction associated with a critical instruction request (Lentz: Figure 7, column 14 lines 32-67 continued to column 15 lines 1-2 and 13-27)(The request with the highest priority is granted over a lower priority request. It would be obvious to one of ordinary skill in the art at the time of the invention that a request with a higher priority is more critical than one with a lower priority).

26. As per claim 4:

Joy, Ebner, Yu, and Lentz disclosed the processing unit of claim 2, wherein the instruction request arbiter increments the priority indication of an unselected instruction request (Lentz: Figure 7, column 15 lines 13-27)(A priority counter is decremented each time a request isn't serviced. This indicates that the request will have a higher priority the next time it's looked at. One of ordinary skill in the art would have realized that the counter could have just as easily be incremented instead of decremented to achieve the same result. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the priority could be incremented instead of decremented to achieve the same result.).

27. As per claim 7:

Joy, Ebner, and Yu disclosed the processing unit of claim 1.

Joy, Ebner, and Yu failed to teach wherein the instruction request arbiter detects the conflicting instruction requests when each instruction request is associated with the same group of cache sets of the instruction memory.

However, Lentz disclosed wherein the instruction request arbiter detects the conflicting instruction requests when each instruction request is associated with the same group of cache sets of the instruction memory (Lentz: Figure 7, column 15 lines 13-27)(The arbiter detects conflicts between row matches for instructions and increments the priority.).

Joy, Ebner, and Yu disclosed an arbiter that will pick between multiple requests for data from the external cache. The data could be either instruction operands or instructions. However, Joy, Ebner, and Yu don't disclose the process of how the arbitration is done. Lentz disclosed an arbiter that specifies how the arbitration is done between multiple requests. One of ordinary skill in the art would have been motivated to add a process of arbitration to the arbiter of Joy to be able to choose between multiple requests. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement an arbiter with a process of arbitration so that a request could be chosen among multiple requests.

28. As per claim 17:

Claim 17 essentially recites the same limitations of claim 2. Therefore, claim 17 is rejected for the same reasons as claim 2.

29. As per claim 19:

Claim 19 essentially recites the same limitations of claim 7. Therefore, claim 19 is rejected for the same reasons as claim 7.

30. As per claim 22:

Claim 22 essentially recites the same limitations of claim 2. Therefore, claim 22 is rejected for the same reasons as claim 2.

31. As per claim 23:

Claim 23 essentially recites the same limitations of claim 3. Therefore, claim 23 is rejected for the same reasons as claim 3.

32. As per claim 24:

Claim 24 essentially recites the same limitations of claim 4. Therefore, claim 24 is rejected for the same reasons as claim 4.

33. As per claim 27:

Claim 27 essentially recites the same limitations of claim 7. Therefore, claim 27 is rejected for the same reasons as claim 7.

34. As per claim 33:

Claim 33 essentially recites the same limitations of claim 2. Therefore, claim 33 is rejected for the same reasons as claim 2.

35. As per claim 34:

Claim 34 essentially recites the same limitations of claim 4. Therefore, claim 34 is rejected for the same reasons as claim 4.

36. As per claim 37:

Claim 37 essentially recites the same limitations of claim 7. Therefore, claim 37 is rejected for the same reasons as claim 7.

37. As per claim 38:

Claim 38 essentially recites the same limitations of claim 3. Therefore, claim 38 is rejected for the same reasons as claim 3.

38. As per claim 44:

Claim 44 essentially recites the same limitations of claim 2. Therefore, claim 44 is rejected for the same reasons as claim 2.

39. As per claim 45:

Claim 45 essentially recites the same limitations of claim 7. Therefore, claim 45 is rejected for the same reasons as claim 7.

40. As per claim 46:

Claim 46 essentially recites the same limitations of claim 3. Therefore, claim 46 is rejected for the same reasons as claim 3.

41. Claims 5-6, 18, 25-26, and 35-36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Joy et al. (U.S. 6,507,862), in view of Ebner et al. (U.S. 6,928,525) and Yu et al. (U.S. 6,345,345), further in view of Thekkath et al. (U.S. 6,490,642).

42. As per claim 5:

Joy, Yu, and Ebner disclosed the processing unit of claim 1.

Joy, Yu, and Ebner failed to teach wherein the instruction request arbiter resolves conflicts between instruction requests having equal priority indications by using

round-robin arbitration.

However, Thekkath disclosed wherein the instruction request arbiter resolves conflicts between instruction requests having equal priority indications by using round-robin arbitration (Thekkath: Figure 1 element 102, column 7 lines 17-39)(The arbiter determines equal priority requests by a round robin scheme.).

Joy, Yu, and Ebner disclosed an arbiter that will pick between multiple requests for data from the external cache. The data could be either instruction operands or instructions. However, Joy, Yu, and Ebner don't disclose the process of how the arbitration is done. Thekkath disclosed an arbiter that specifies how the arbitration is done between multiple requests. One of ordinary skill in the art would have been motivated to add a process of arbitration to the arbiter of Joy to be able to choose between multiple requests. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement an arbiter with a process of arbitration so that a request could be chosen among multiple requests.

43. As per claim 6:

Claim 6 essentially recites the same limitations of claim 4. Therefore, claim 6 is rejected for the same reasons as claim 4.

44. As per claim 18:

Claim 18 essentially recites the same limitations of claim 5. Therefore, claim 18 is rejected for the same reasons as claim 5.

45. As per claim 25:

Claim 25 essentially recites the same limitations of claim 5. Therefore, claim 25 is rejected for the same reasons as claim 5.

46. As per claim 26:

Claim 26 essentially recites the same limitations of claim 4. Therefore, claim 26 is rejected for the same reasons as claim 4.

47. As per claim 35:

Claim 35 essentially recites the same limitations of claim 5. Therefore, claim 35 is rejected for the same reasons as claim 5.

48. As per claim 36:

Claim 36 essentially recites the same limitations of claim 4. Therefore, claim 36 is rejected for the same reasons as claim 4.

49. Claims 10-11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Joy et al. (U.S. 6,507,862), in view of Ebner et al. (U.S. 6,928,525) and Yu et al. (U.S. 6,345,345), further in view of O'Dowd (U.S. 5,235,595) and Brauchle et al. (U.S. 5,555,152).

50. As per claim 10:

Joy and Ebner disclosed the processing unit of claim 1.

Joy and Ebner failed to teach an instruction request bus, coupled to a second instruction request arbiter output, coupled the plurality of processor cluster outputs, and coupled to the instruction request arbiter input, the instruction request bus comprising a plurality of flip flops to pipeline the instruction requests and the traffic mode.

However, O'Dowd and Brauchle disclosed an instruction request bus, coupled to a second instruction request arbiter output, coupled the plurality of processor cluster outputs, and coupled to the instruction request arbiter input, the instruction request bus comprising a plurality of flip flops to pipeline the instruction requests (O'Dowd: Figure 1 element 12, column 7 lines 60-67 continued to column 8 lines 1-20)(Brauchle: Column 1 lines 56-67 continued to column 2 lines 1-5)(O'Dowd disclosed a single direction bus containing switch elements. Brauchle disclosed switching elements being flip-flops.).

The advantage of using a bus containing flip-flops is that it allows for the high speed transfer and low latency delays of packets (O'Dowd: Column 7 lines 9-15). One of ordinary skill in the art would have been motivated by increased speed in packet transfers to implement the single directional bus with switch elements for packet transfers. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a single directional bus with switch elements for packet transfers for the benefit of increased transfer speed.

Joy, Ebner, O'Dowd, and Brauchle failed to teach the instruction request bus comprising a traffic mode.

However, Yu disclosed the instruction request bus comprising a traffic mode (Yu: Figure 4, column 7 lines 20-53)(The traffic mode is determined on whether the number of transfers are limited or not).

The advantage of the arbitration system of Yu is that data traffic conditions can be monitored dynamically (Yu: Column 1 lines 46-48). Control values can be set that limits the amount of traffic of data transfers in a given clock cycle (Yu: Column 2 lines 6-

13). One of ordinary skill in the art at the time of the invention would have implemented the arbitration system of Yu for the advantage of dynamically monitoring data traffic to the system's memory. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement Yu's arbitration system for the advantage of dynamically monitoring and determining the amount of data traffic allowable to the system's memory.

51. As per claim 11:

Joy, Ebner, O'Dowd, Brauchle, and Yu disclosed the processing unit of claim 10, wherein the instruction request bus comprises a slotted ring (O'Dowd: Figure 1 element 12, column 7 lines 60-67 continued to column 8 lines 1-20)(A slotted ring is a bus that is only one directional. The bus in figure one is one directional with intervening flip-flops.).

52. Claims 12, 20, and 48 are rejected under 35 U.S.C. §103(a) as being unpatentable over Joy et al. (U.S. 6,507,862), in view of Ebner et al. (U.S. 6,928,525) and Yu et al. (U.S. 6,345,345), further in view of Bass et al. (U.S. 6,769,033).

53. As per claim 12:

Joy and Ebner disclosed the processing unit of claim 1.

Joy and Ebner failed to teach wherein the processing unit comprises a network processor and the instruction data comprises packet processing instructions related to at least one from the group consisting of: packet routing, switching, bridging, and forwarding.

However, Bass disclosed wherein the processing unit comprises a network

processor (Bass: column 4 lines 47-63) and the instruction data comprises packet processing instructions related to at least one from the group consisting of: packet routing, switching, bridging, and forwarding (Bass: Column 5 lines 20-32)(The network processor performs packet switching).

The advantage of using a network processor is that they can increase bandwidth and solve latency problems by executing network operations in hardware (Bass: Column 2 lines 63-67 continued to column 3 lines 1-25). One of ordinary skill in the art would have been motivated to implement a network processor for the advantage of increased bandwidth and performance. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the processor of Joy as a network processor for the advantage of increased bandwidth and performance.

54. As per claim 20:

Claim 20 essentially recites the same limitations of claim 12. Therefore, claim 20 is rejected for the same reasons as claim 12.

55. As per claim 48:

Claim 48 essentially recites the same limitations of claim 12. Therefore, claim 48 is rejected for the same reasons as claim 12.

Response to arguments

56. The arguments presented by Applicant in the response, received on 7/10/2006 are not considered persuasive.

57. Applicant argues that "Claims 1 and 16 incorporate parts of dependent allowable claims that Joy and Ebner don't disclose."

This argument is found to be persuasive for the following reason. The examiner agrees that Joy and Ebner don't disclose the newly added limitation from claim 8 that was previously deemed allowable if written into independent form. However, since all of the limitations of claim 8 weren't incorporated into claims 1 and 16, a new grounds of rejection has been given to the claims. The combination of Yu, with Joy and Ebner results in an arbiter that controls traffic between processing clusters. Yu disclosed implementing a limit of transfers from one space to another, and implementing a wait signal if the transfer limit is reached, which stops all traffic from one space to another. Thus, the combination results in the arbiter controlling data transfers according to the traffic mode of either transferring data or waiting because data transfers have exceeded a limit.

58. Applicant argues that "Claims 21, 32, and 43 incorporate parts of dependent allowable claims that aren't disclosed by either Joy, Ebner, or Yu."

This argument is not found to be persuasive for the following reason. Since all of the limitations of claim 8 weren't incorporated into claims 21, 32, and 43, a new grounds of rejection has been given to the claims. The combination of Yu, with Joy and Ebner results in an arbiter that controls traffic between processing clusters. Yu disclosed implementing a limit of transfers from one space to another, and implementing a wait signal if the transfer limit is reached, which stops all traffic from one space to another. Thus, the combination results in the arbiter controlling data transfers according to the

traffic mode of either transferring data or waiting because data transfers have exceeded a limit.

Allowable Subject Matter

59. Claims 8-9, 28-29, and 39-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183

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